Trapping processes in vertical GaN Trench MOSFETs: from experimental analysis to simulations

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In the past years, Gallium Nitride (GaN) has emerged as an excellent semiconductor material for the realization of power devices, especially thanks to the high critical electric field, high electron mobility. Currently, most of the GaN devices in the market consist of AlGaN/GaN HEMTs, lateral transistors in which the channel consist of a 2-dimension electron gas obtained thanks to the piezoelectric polarization charges. Vertical GaN (v-GaN) devices are currently under development for the realization of high voltage power devices that overcome the intrinsic limitations of the lateral structures [1]. In particular, GaN-on-Si is expected to provide a cost-effective alternative to Si-based power MOSFETs.

In this presentation, we will discuss on the charge trapping mechanisms leading to threshold voltage instability in ON-state condition in vertical GaN-on-Si trench MOSFETs obtained with a fully-compatible CMOS process that employ SiO_2 as gate dielectric. First, we will describe the custom experimental technique developed for the analysis of V_{TH} instability. Then, we will develop a trapping model based on basic tunnelling equations [2]. Finally, the model was validated by TCAD simulations capable of reproducing the experimental data [3].

The results shown here identify as a root cause for the V_{TH} instability the presence of border traps in the oxide layer, that can be easily accessed by the electrons with elastic tunnelling processes.

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References

[1] M. Meneghini *et al.*, "GaN-based power devices: Physics, reliability, and perspectives," *J Appl Phys*, vol. 130, no. 18, p. 181101, Nov. 2021, doi: 10.1063/5.0061354.

[2] M. Fregolent *et al.*, "Threshold voltage instability in SiO2-gate semi-vertical GaN trench MOSFETs grown on silicon substrate," *Microelectronics Reliability*, vol. 150, p. 115130, Nov. 2023, doi: 10.1016/j.microrel.2023.115130.

[3] N. Zagni *et al.*, "Physical insights into trapping effects on vertical GaN-on-Si trench MOSFETs from TCAD," *Journal of Semiconductors*, vol. 45, no. 3, p. 032501, Mar. 2024, doi: 10.1088/1674-4926/45/3/032501.